a circuit component of an integrated circuit provided in one of said active areas, and connected between said terminal and a first source of constant voltage; and

a protection circuit provided in at least said one of said active areas, and comprising:

a first impurity region of said one conductivity type [provided under] said at least one of said active areas, wherein said first impurity region is a base region of a bipolar transistor,

a second impurity region of the other conductivity type opposite to said one conductivity type provided in a surface portion of said first impurity region, connected to said terminal, wherein said second impurity region is one of an emitter region and a collector region of said bipolar transistor; and

a third impurity region of said other conductivity type connected to said first source of constant voltage, provided in another surface portion of said semiconductor substrate, wherein said third impurity region is the other of said emitter region and said collector region of said bipolar transistor.

2. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein said third impurity region further comprises:

a first impurity sub-region provided in a surface portion of another active area adjacent to said one of said active areas; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

3. (*Amended*) The semiconductor integrated circuit device as set forth in claim 2, wherein said first impurity sub-region comprises:

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

4. (*Amended*) The semiconductor integrated circuit device as set forth in claim 2, wherein said circuit component is a field effect transistor comprising source and drain regions of said other conductivity type provided in said one of said active areas, and one of said source and drain regions is said second impurity region.

5. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein said third impurity region comprises:

a first impurity sub-region provided in another surface portion of said first impurity region spaced from said second impurity region; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

6. (*Amended*) The semiconductor integrated circuit device as set forth in claim 5, wherein said first impurity sub-region comprises:

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

7. (*Amended*) The semiconductor integrated circuit device as set forth in claim 5, wherein said circuit component is a field effect transistor comprising source and drain regions of said other conductivity type provided in said one of said active areas, wherein one of said source and drain regions is said second impurity region, and the other of said source and drain regions is said first impurity sub-region.

8. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein said third impurity region is provided in another active area adjacent to said one of said active areas and having a second depth greater than said first depth.

9. (*Amended*) The semiconductor integrated circuit device as set forth in claim 8, wherein said circuit component is a field effect transistor comprising source and drain regions of said other conductivity type provided in said one of said active areas, and one of said source and drain regions is said second impurity region.

10. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein said third impurity region is provided in another surface portion of said first impurity region and deeper than said second impurity region.

11. (*Amended*) The semiconductor integrated circuit device as set forth in claim 10, wherein said circuit component is a field effect transistor comprising source and drain regions of said other conductivity type provided in said one of said active areas, one of said source and drain regions is said second impurity region, and the other of said source and drain region is a part of said third impurity region.

12. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein said third impurity region extends in said first impurity region under said second impurity region.

13. (*Amended*) The semiconductor integrated circuit device as set forth in claim 10, wherein said circuit component is a field effect transistor comprising source and drain regions of said other conductivity type provided in said one of said active areas, and one of said source and drain regions is said second impurity region.

14. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein said terminal is a signal output terminal, and said circuit component is an output transistor.

15. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein said terminal is a signal input and output terminal, and said circuit component is an output transistor comprising a portion of an input and output circuit connected to said terminal.

Please add the following new claims:

17. (*New*) A semiconductor integrated circuit device provided on a semiconductor substrate of a first conductivity type, comprising:

a plurality of active areas provided in a portion of said semiconductor substrate;

at least one shallow trench isolation region disposed between said active areas;

a terminal connected to one of said active areas;

a circuit component connected between said terminal and a first source of constant voltage; and

a protection circuit provided in at least said one of said active areas, said protection circuit comprising:

a first impurity region of said first conductivity type provided under at least one of said active areas and serving as a base region of a bipolar transistor,

a second impurity region of a second conductivity type opposite to said first conductivity type provided in said active area connected to said terminal, and serving as one of an emitter region and a collector region of said bipolar transistor; and

a third impurity region of said second conductivity type connected to said first source of constant voltage, provided in another portion of said semiconductor substrate and serving as the other of said emitter region and said collector region of said bipolar transistor.

18. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein said circuit component is a field effect transistor.

19. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein said third impurity region further comprises:

a first impurity sub-region provided in a surface portion of an active area adjacent to said at least one shallow trench isolation region; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region.

20. (*New*) The semiconductor integrated circuit device as set forth in claim 18, wherein said first impurity sub-region comprises a first portion contiguous to said second impurity sub-region.

21. (*New*) The semiconductor integrated circuit device as set forth in claim 20, wherein said first impurity sub-region further comprises a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

22. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein said at least one shallow trench isolation region has a first depth and said third impurity region has a second depth greater than said first depth.

23. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein the depth of said third impurity region is deeper than the depth of said second impurity region.

24. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein said third impurity region extends into said first impurity region under said second impurity region.

25. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein an upper surface of said third impurity region is contiguous with a bottom surface of said first impurity region.

26. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein said first impurity region is a p-type impurity region.

27. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein said second impurity region is a n-type impurity region.

28. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein said third impurity region is a n-type impurity region.

29. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein said terminal is a signal output terminal and said circuit component is an output transistor.

30. (*New*) The semiconductor integrated circuit device as set forth in claim 17, wherein said terminal is a signal input and output terminal, and said circuit component is an output transistor comprising a portion of an input and output circuit connected to said terminal.